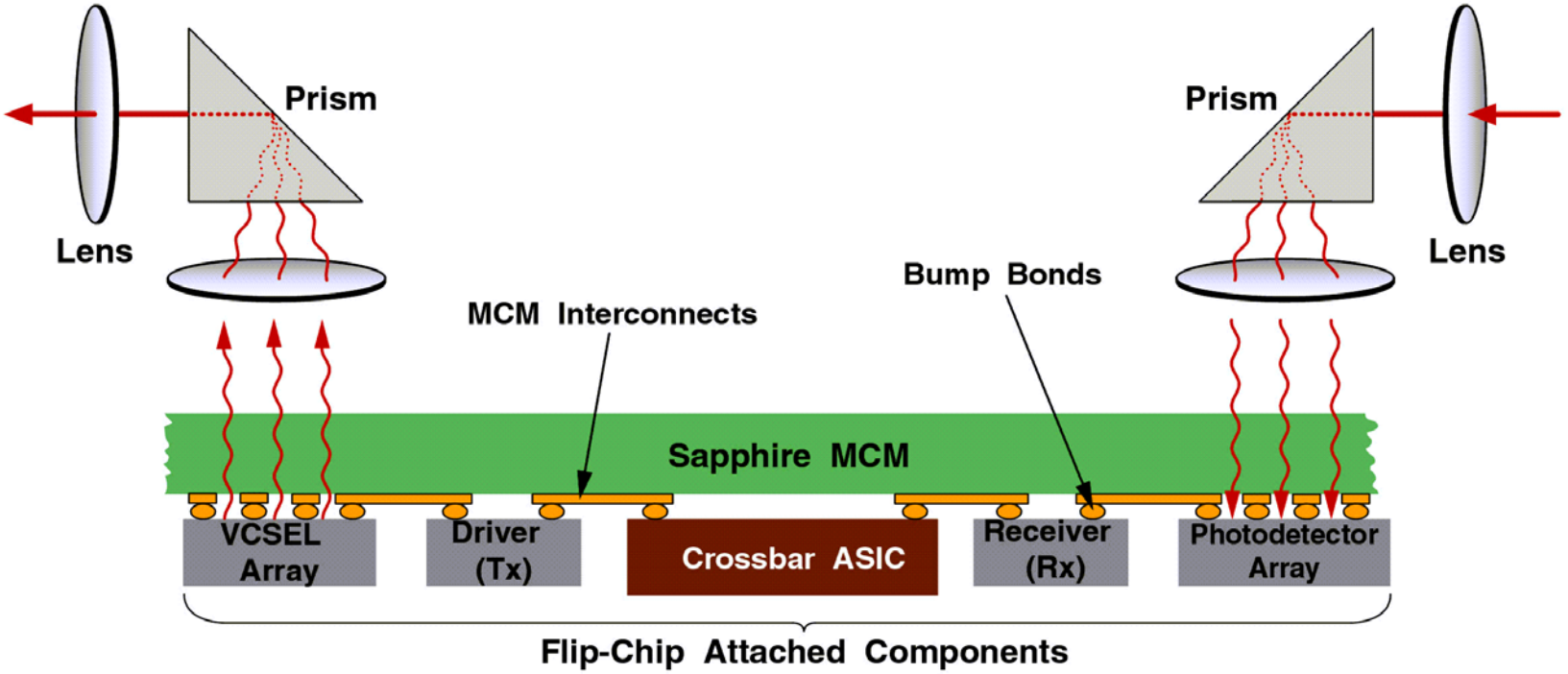
MAYO INVOLVEMENT IN DARPA/MTO VLSI PHOTONICS PROGRAM

Sponsor: D. Radack, DARPA/MTO
Presented By: Gregg Fokken
Mayo Foundation
July 30, 2001

OVERVIEW

- **Focused on three separate efforts under VLSI Photonics Program**
  - **Northrop Grumman Team: Non-blocking crossbar switch implemented as a backplane.**
  - **Honeywell VIVACE Team: Non-blocking crossbar switch implemented as a switch module.**
  - **University of Deleware Team: High per-channel data rate free space optics demonstration.**

CROSS SECTION AND TASK BREAKDOWN FOR NORTHROP GRUMMAN FREE SPACE OPTICAL INTERCONNECT DEMONSTRATION UNDER VLSI PHOTONICS PROGRAM
(Mayo Tx/Rx ASICs Designed in Honeywell 0.35 μm CMOS Silicon-On-Insulator (SOI) Technology)



Breakdown Of Mayo Tasks

- Design of 4-Channel Driver (Tx) and Receiver (Rx) ASICs for Interim Demonstration
- Sapphire MCM Interconnect Modeling and Design Advice
- Crossbar to Tx, and Rx to Crossbar Low-Power, High-Speed I/O Design

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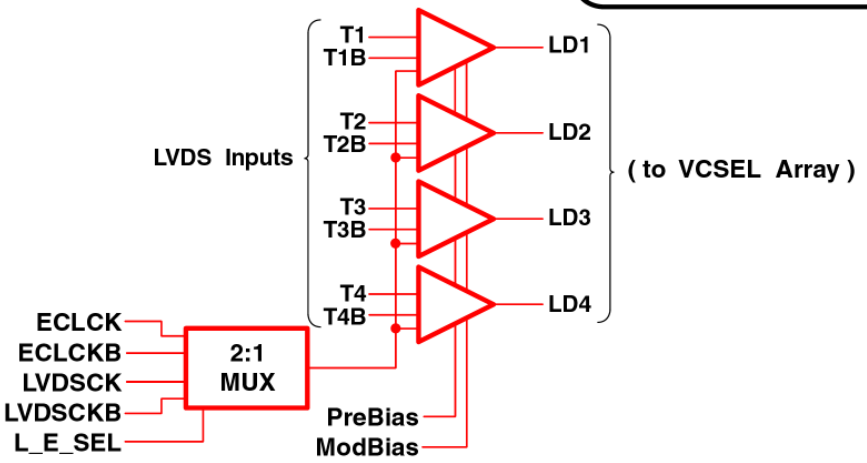
BLOCK DIAGRAM AND CAD LAYOUT OF NORTHROP GRUMMAN 4-CHANNEL OPTOELECTRONIC TRANSMITTER AND RECEIVER CIRCUITS IMPLEMENTED BY MAYO IN HONEYWELL 0.35 μm CMOS SOI

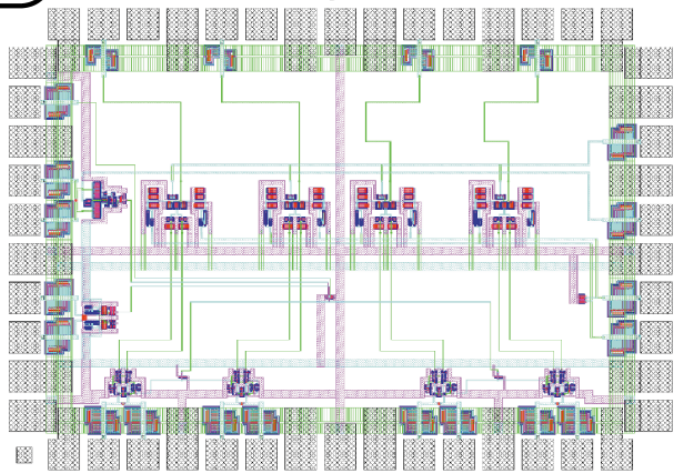
(Designed for Synchronously Driving and Receiving Signals from VCSEL and Photodetector Arrays at >1 Gb/s per Channel Data Rates; LVDS or PECL Clock Inputs; Tape-Out, 12/99)

4-Channel Transmitter

Block Diagram

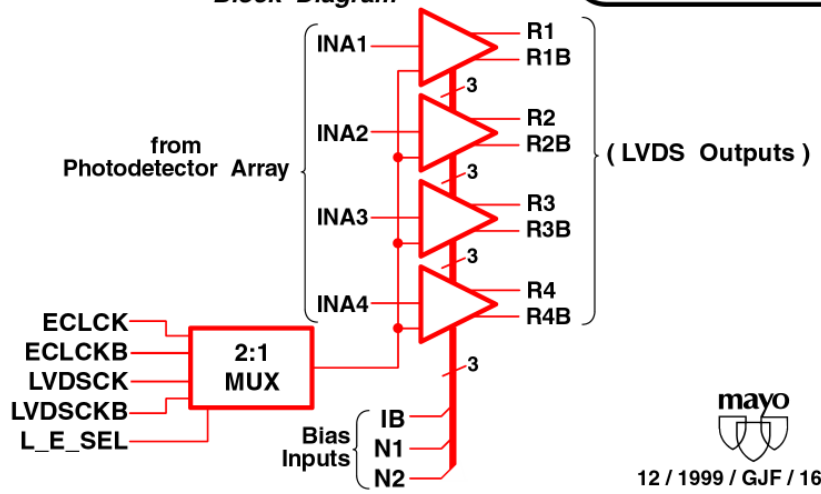


Layout

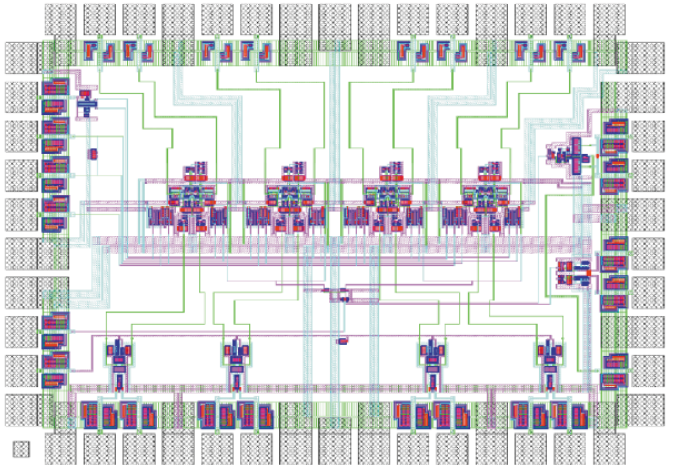


4-Channel Receiver

Block Diagram



Layout



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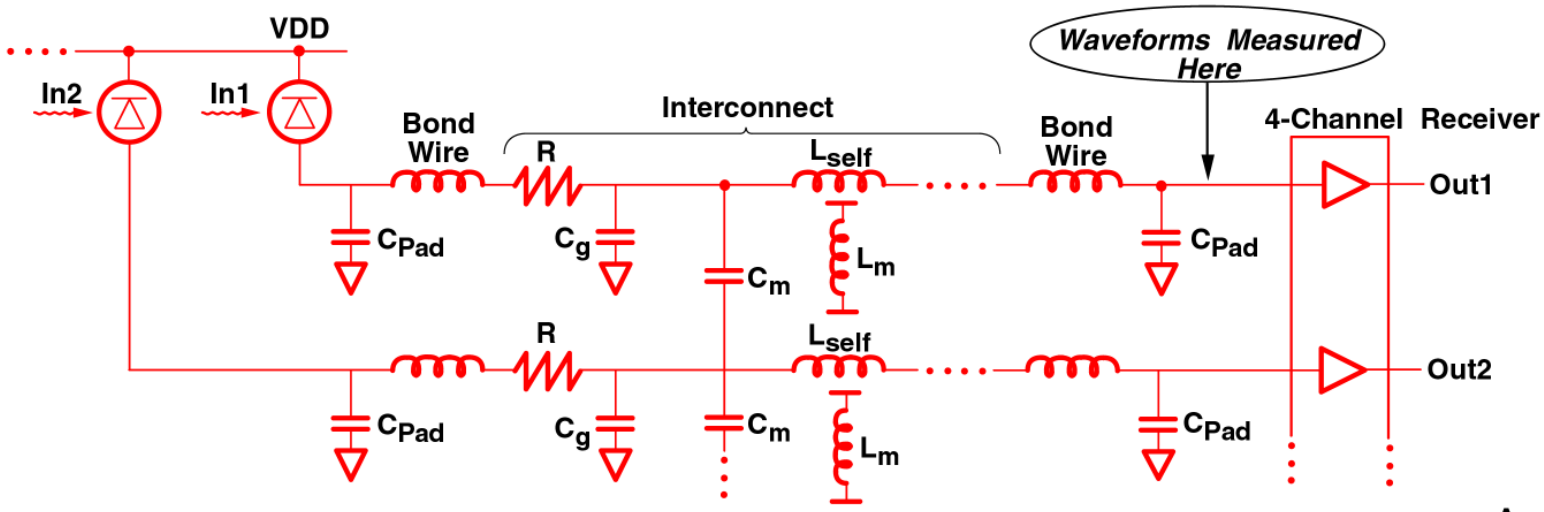
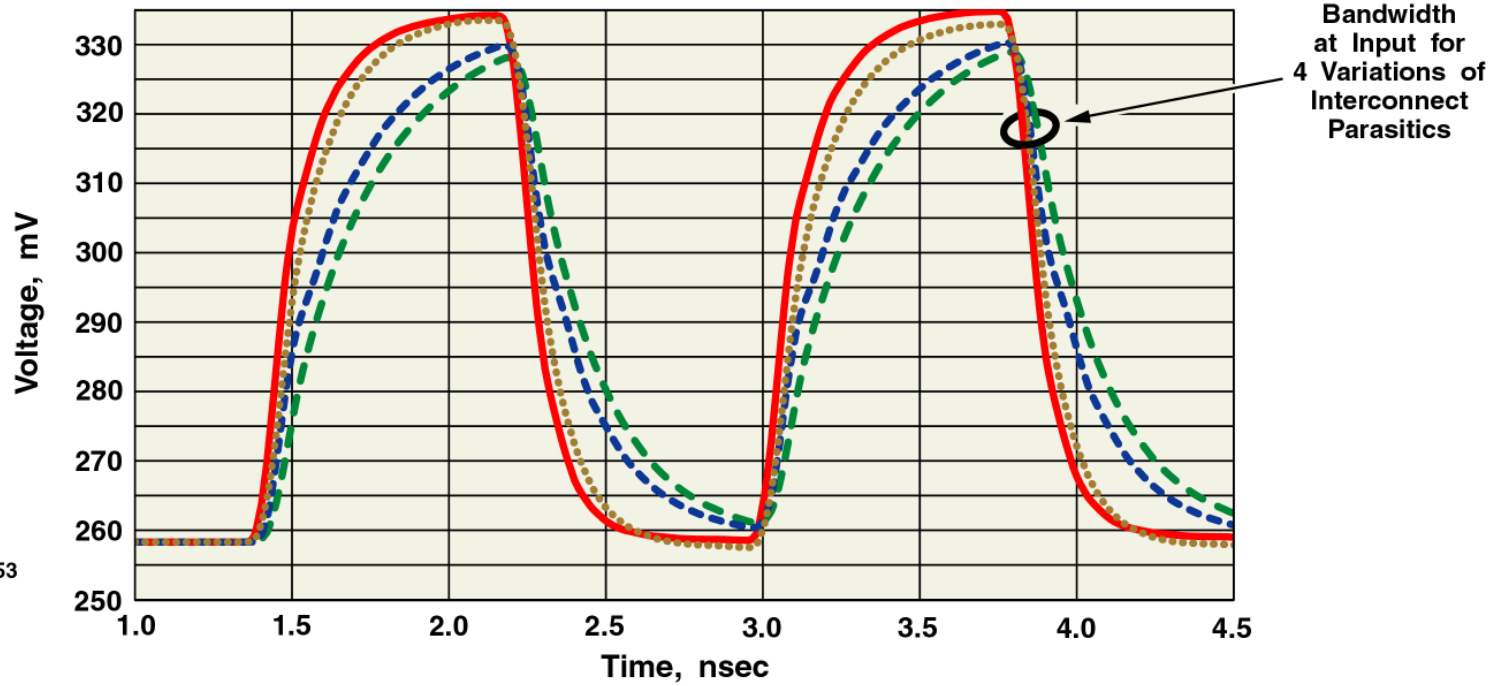
EXAMPLE OF SIGNAL INTEGRITY MODELING OF NORTHROP GRUMMAN OPTOELECTRONIC RECEIVER FOR VLSI PHOTONICS PROGRAM

(Modeled in HSPICE Using Honeywell 0.35 μm CMOS SOI Models for Receiver and Distributed RLC Models for Interconnect Parasitics)





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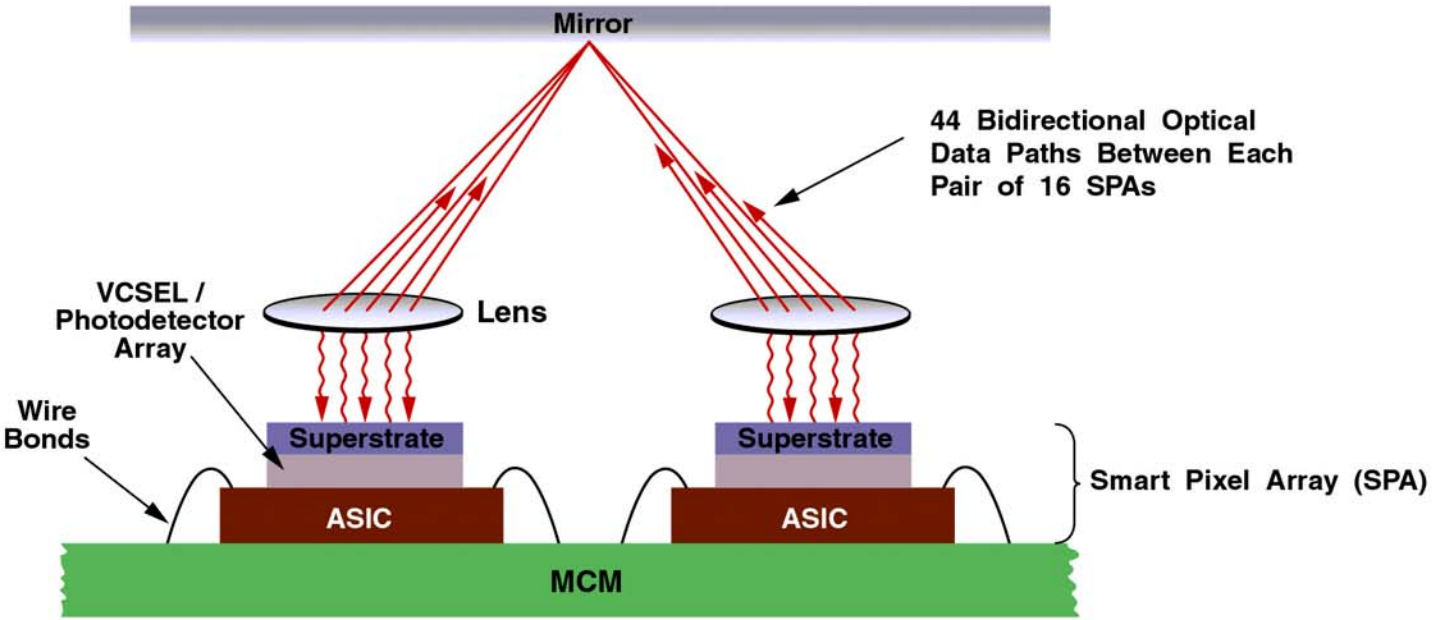
CROSS SECTION VIEW OF FREE SPACE OPTICAL INTERCONNECTS DEMONSTRATION AND MAYO TASK BREAKDOWN FOR VIVACE COLLABORATION UNDER DARPA/MTO VLSI PHOTONICS PROGRAM

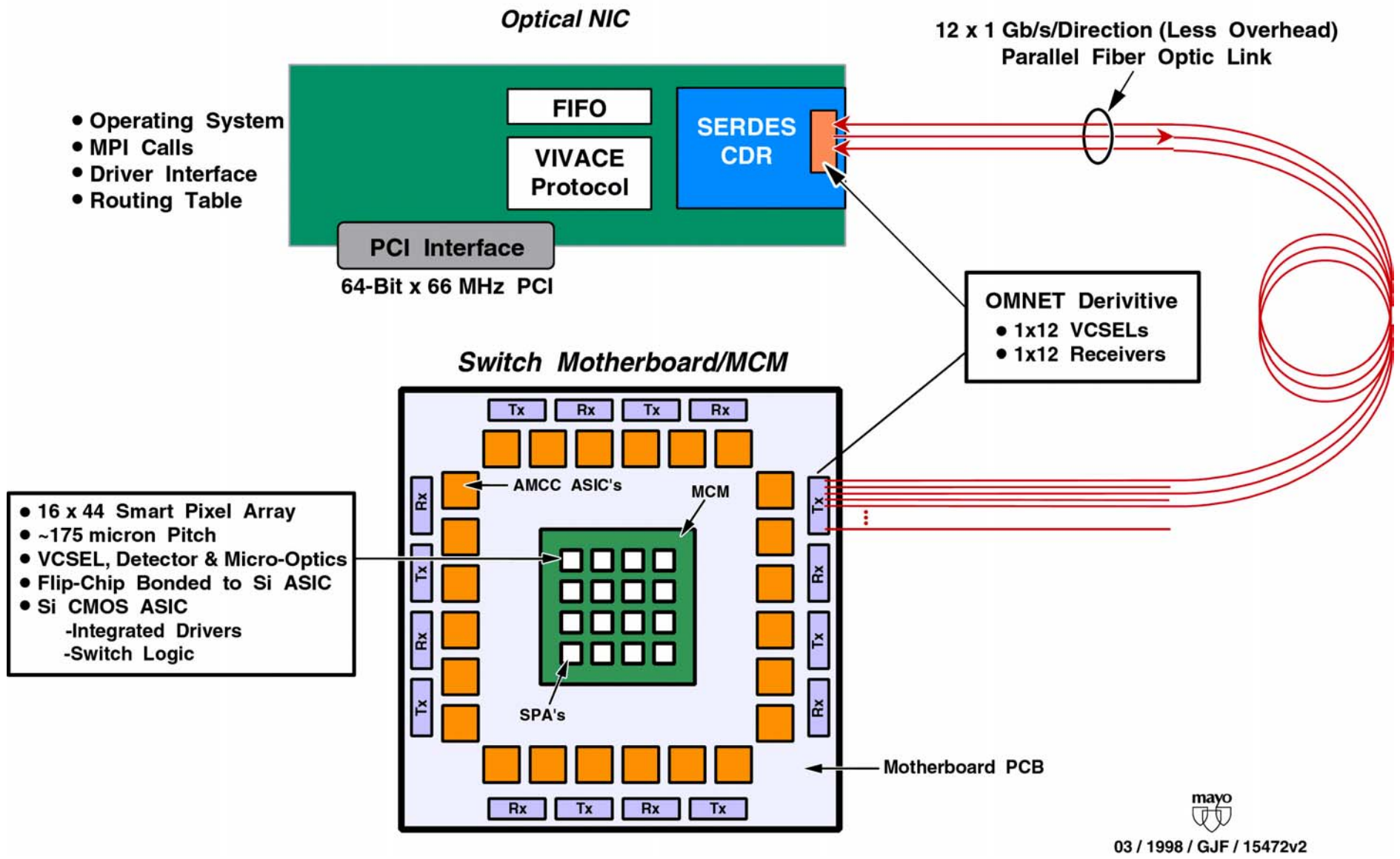


Task Breakdown:

- Development of Switch MCM
  - Mechanical Analysis
  - Thermal Analysis
  - MCM Design and Layout
  - MCM Fabrication (currently planned for MCM-C vendor)
  - Precision MCM Assembly
  - Initial Test
- Signal Integrity (SI) and Simultaneous Switching Noise (SSN) analysis on-chip, on-MCM, and on-motherboard

BLOCK DIAGRAM OF VIVACE SYSTEM DEMONSTRATION UNDER DARPA/MTO VLSI PHOTONICS PROGRAM

(Multiple Network Interface Cards (NICs) Would Interface to Each Other Through Non-Blocking Crossbar Switch MCM Using Free Space Optical Interconnects)



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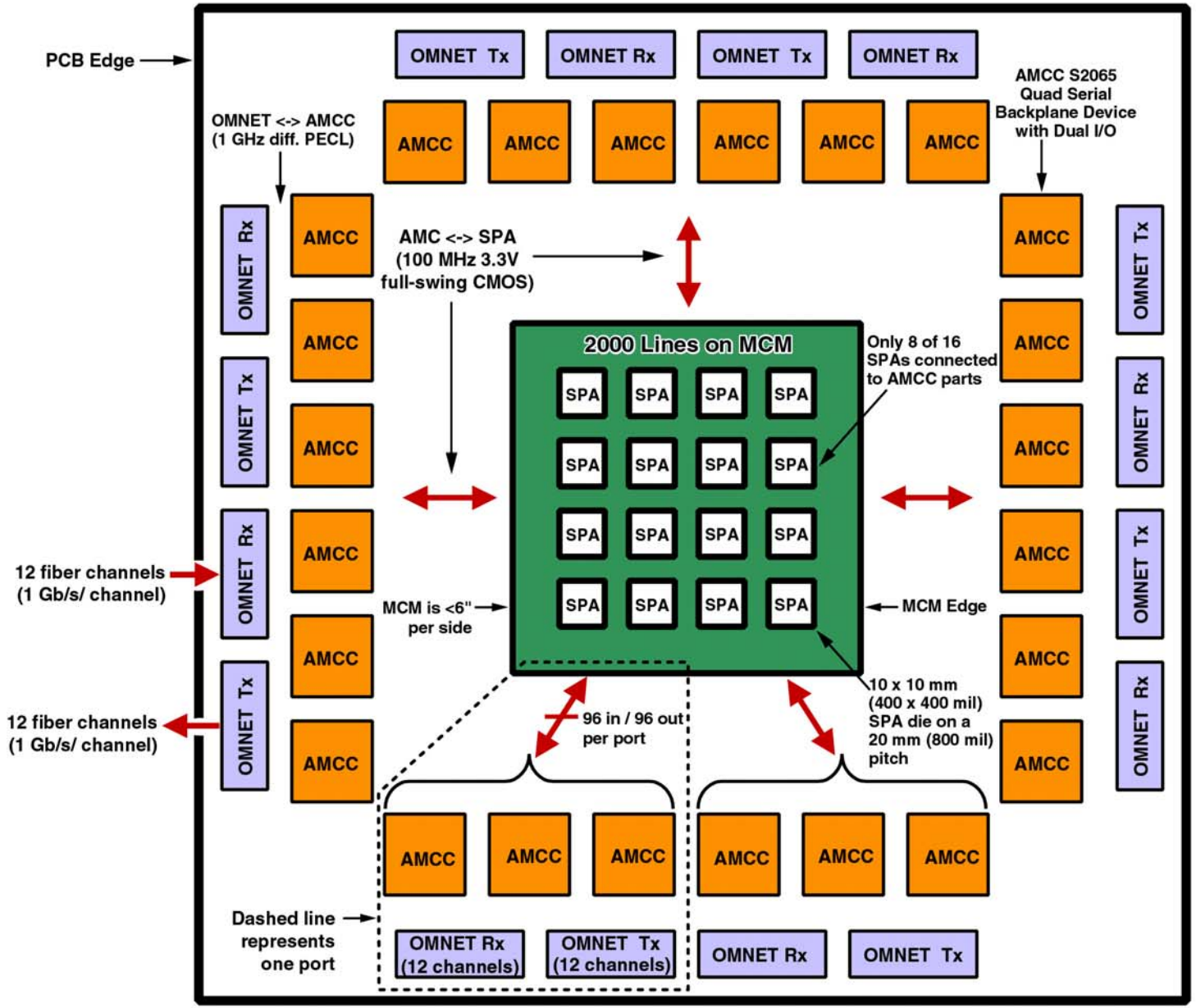
CONCEPTUAL DRAWING OF VIVACE TEAM SWITCH MCM AND PCB IMPLEMENTED UNDER DARPA/MTO VLSI PHOTONICS PROGRAM

(Switch MCM is Designed as an 8 Port Non-Blocking Crossbar Switch Where All Smart Pixel Arrays (SPAs) Are Interconnected Through Free Space Optics)



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Not to Scale

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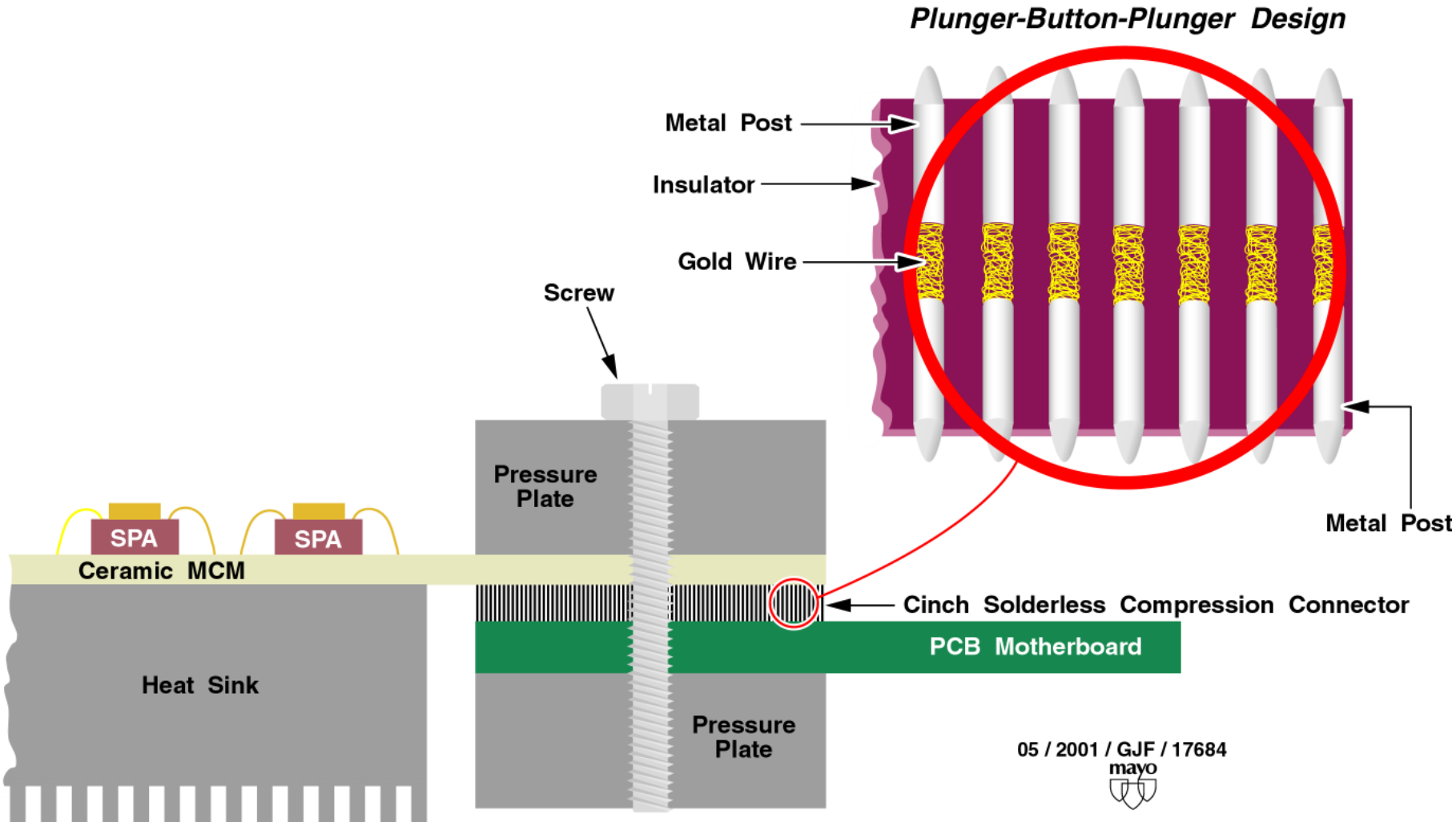
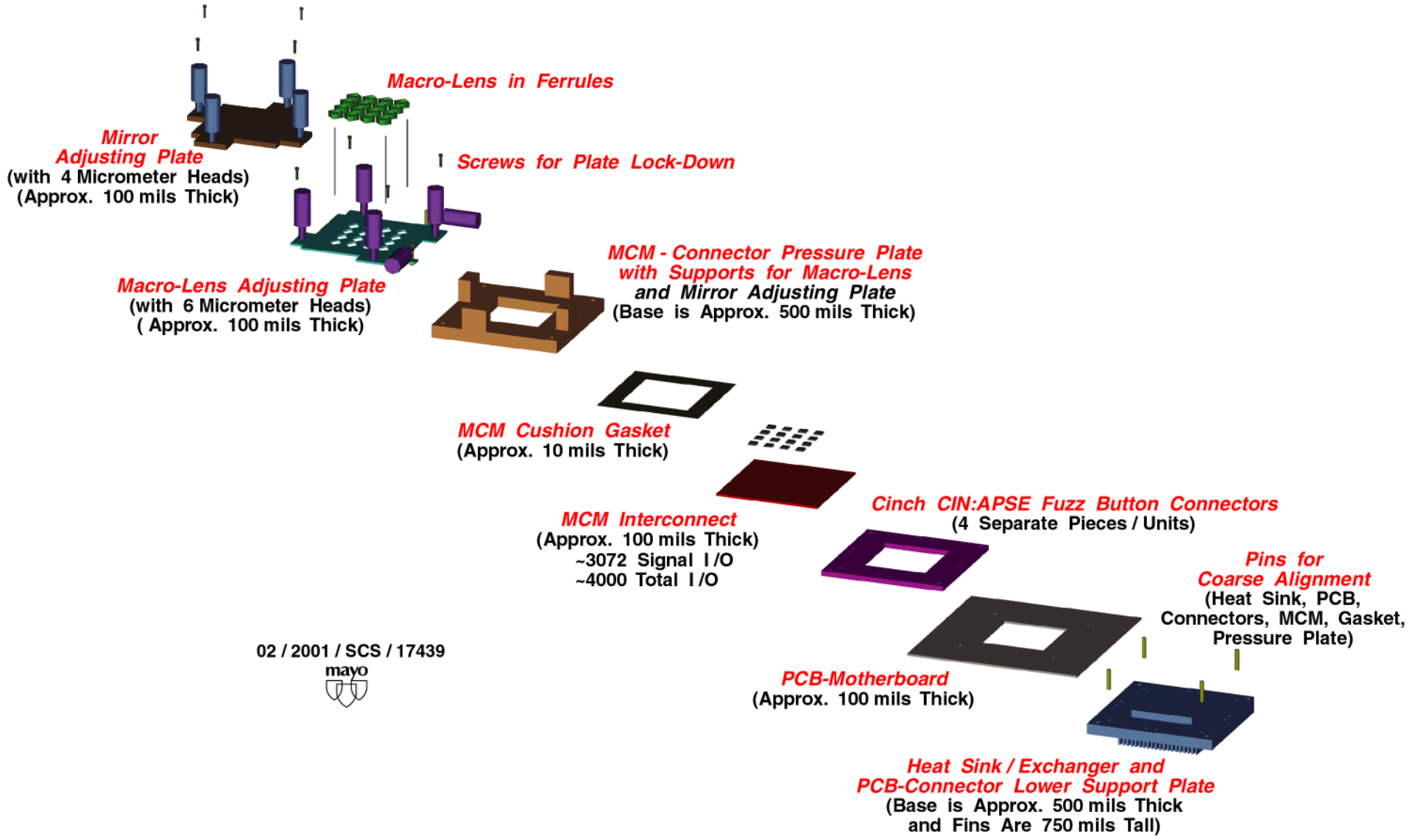
CROSS SECTION VIEW OF SWITCH MCM, CINCH SOLDERLESS COMPRESSION CONNECTOR, AND PCB MOTHERBOARD USED IN VIVACE FREE SPACE OPTICAL INTERCONNECTS DEMONSTRATION

(MCM Contains 16 Smart-Pixel-Arrays with All Chip-to-Chip Communication Through Free Space Optical Links; Cinch CIN:APSE Connector Contains ~4000 Signal, Power, and Ground Connections)



VLSI PHOTONICS PROGRAM - VIVACE AUTOCAD SOLID MODEL DRAWING; PROPOSED MECHANICAL INTEGRATION / ASSEMBLY OF COMPONENTS

(Mechanical Design and Assembly for Integration of the Optical Lenses, Mirror, MCM, Dematable Connector, PCB, and Heat Sink/Exchanger; AUTOCAD R14 Solid Model Rendered in 3D; Exploded View of Assembly)



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VLSI PHOTONICS PROGRAM - VIVACE ANSYS MODEL SIMULATION OF STRUCTURAL DEFORMATION OF MCM-CONNECTOR PRESSURE PLATE

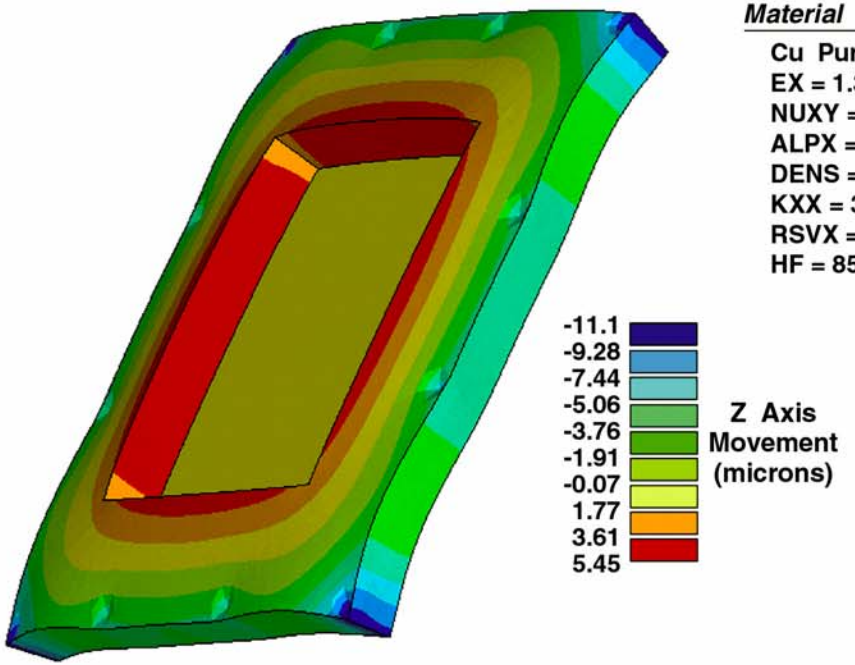
(Deformation of MCM-Connector Pressure Plate Contacting Top Side Periphery of MCM Providing Compression Force to Connect Cinch Corporation, Fuzz Button Plungers Between Motherboard PCB and MCM Backside; ~4000 Connections From MCM to Motherboard PCB Around MCM Perimeter; ~1000 lbs Force to Compress All Fuzz Button Connections)

0.5" Thick

Z Axis Deflection Scale:

-11.1 microns *to* 5.45 microns

Force at Each of 12 Nodes: 810N



Material Parameters

Cu Pure
EX = 1.38E+11
NUXY = .35
ALPX = 17.1E-06
DENS = 8940
KXX = 390
RSVX = 1.7E-08
HF = 85.174

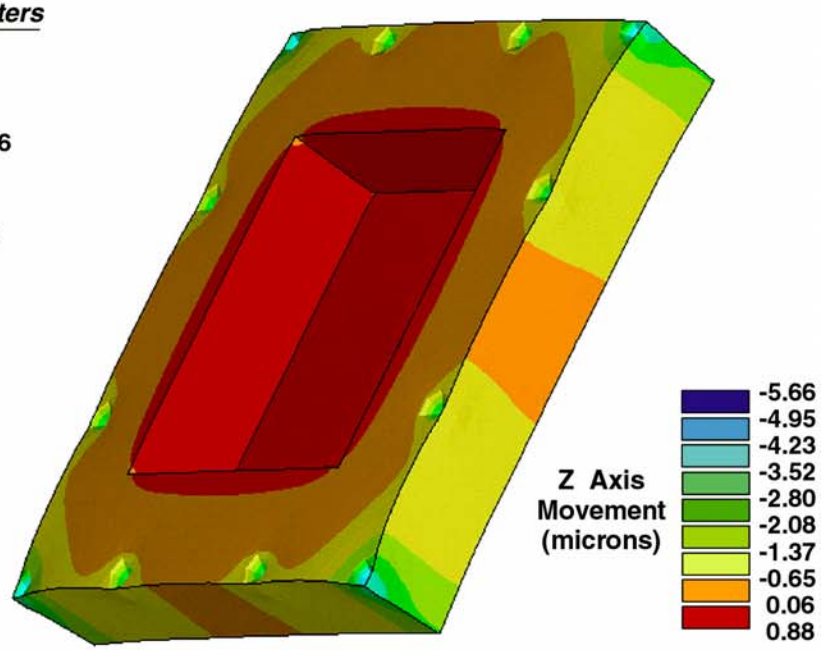
0.0127 m Thick and 0.1524 m Square Cu Plate (0.5" Thick and 6" Square)

1.0" Thick

Z Axis Deflection Scale:

-5.66 microns *to* 0.777 microns

Force at Each of 12 Nodes: 810N



0.0254 m Thick and 0.1524 m Square Cu Plate (1.0" Thick and 6" Square)

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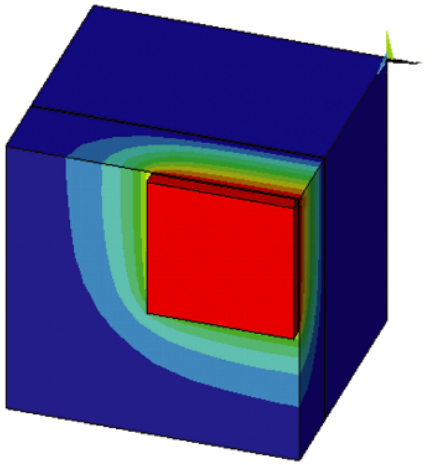
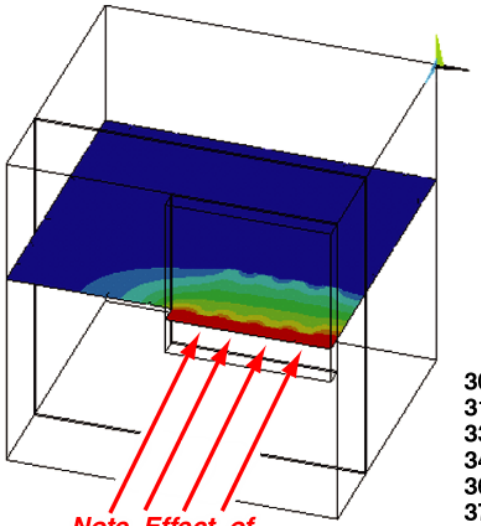
VLSI PHOTONICS PROGRAM - VIVACE ANSYS THERMAL MODEL CROSS SECTION; EFFECTS OF THERMAL VIA CONDUCTIVITY IN CERAMIC MCM

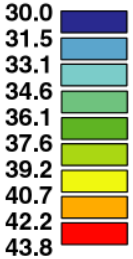
(Finite Element Simulation of Proposed MCM Design; Model Includes Material Definitions for Layer Stack: Cu Heat Sink, 0.003" Thick Diamond Filled Thermoplastic Dry Film Die Attach Adhesive, Low Temperature Cofired Ceramic (LTCC) with 4x4 Thermal Via Array with Two Thermal Conductivities Simulated, Diamond Filled Die Attach, and Si Die; Constant 30° C Maintained on Back of Heat Sink; 10 Watt Heat Flux on Die Face)



Note Only 1/4 of Die Area Modeled; Only a 4 x 4 Array of Vias Shown

Via Thermal Conductivity: 390 W/m-K (Approximately That of Pure Cu)





Average Temperature (°C)

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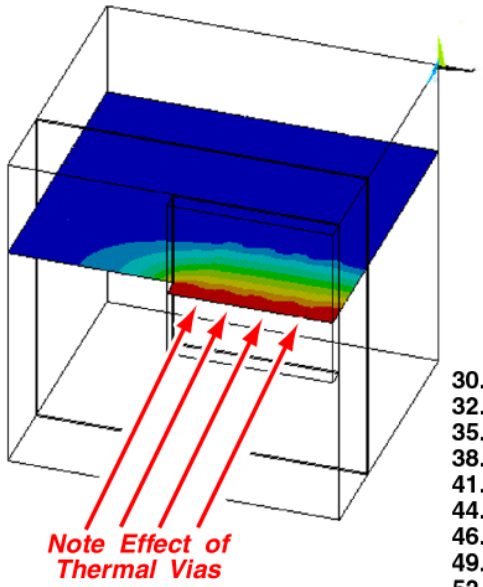
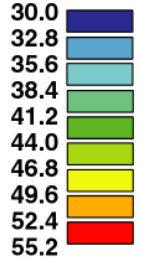
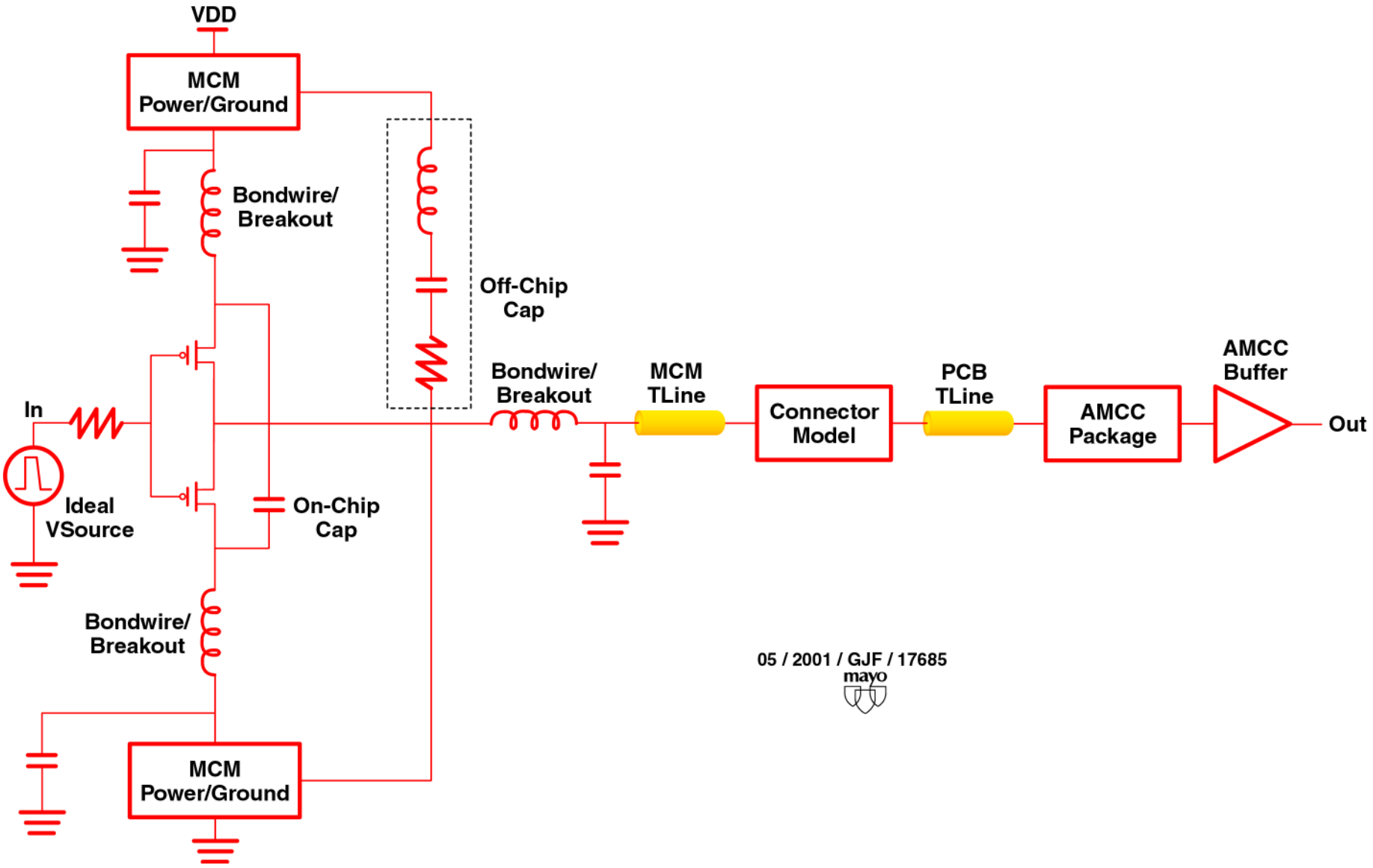
Via Thermal Conductivity: 100 W/m-K





Average Temperature (°C)

BLOCK DIAGRAM OF SIMULTANEOUS SWITCHING NOISE (SNN) MODEL OF SWWITCH MCM USED IN VIVACE FREE SPACE OPTICAL INTERCONNECTS DEMONSTRATION (MCM Contains 16 Smart-Pixel-Arrays (SPAs) with All Chip-to-Chip Communication Through Free Space Optical Links; Each SPA Has 96 Electrical Inputs and 96 Electrical Outputs Potentially Switching Simultaneously)



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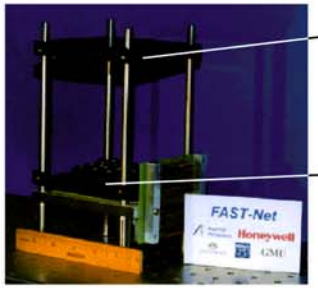
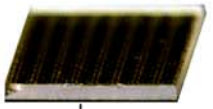
CONCEPTUAL DRAWING OF HIGH SPEED FREE SPACE OPTICAL INTERCONNECTS DEMONSTRATION WITH 10 Gb/s/CHANNEL TARGET DATA RATES IMPLEMENTED UNDER DARPA/MTO VLSI PHOTONICS PROGRAM

Free Space Optics Provided by Applied Photonics / George Mason University



Gallium Arsenide VCSEL/Photodetector Area Arrays and Heterogenous Integration Provided by Honeywell Technology Center



To:
Mayo Hewlett Packard
70843A 12 Gb/s
Bit Error Rate Tester

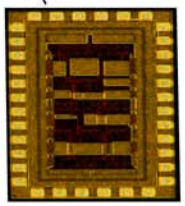
High Performance MCM Design, Assembly, and Test Provided by Mayo Foundation

GOALS

- Characterize Maximum per Channel Data Rates of VCSEL/Photodetector Area Arrays Driven by High Speed CMOS and Bipolar Circuits
- Minimize per Channel Power Consumption (Scalable)

FEATURES

- 10 Gb/s/Channel Target Data Rate (Bipolar Circuits)
- Current-Source and Voltage-Source Drivers (Tx)
- Synchronous and Asynchronous Channels
- On-Chip Linear Feedback Shift Register for Optional On-Chip Pattern Generation
- Designed for Testability, Tailored for Analysis
- IBM SiGe BiCMOS (0.18 μm CMOS, 120 GHz fT Bipolar) Process



High Speed IBM SiGe ASIC Design Provided by University of Delaware and Mayo Foundation

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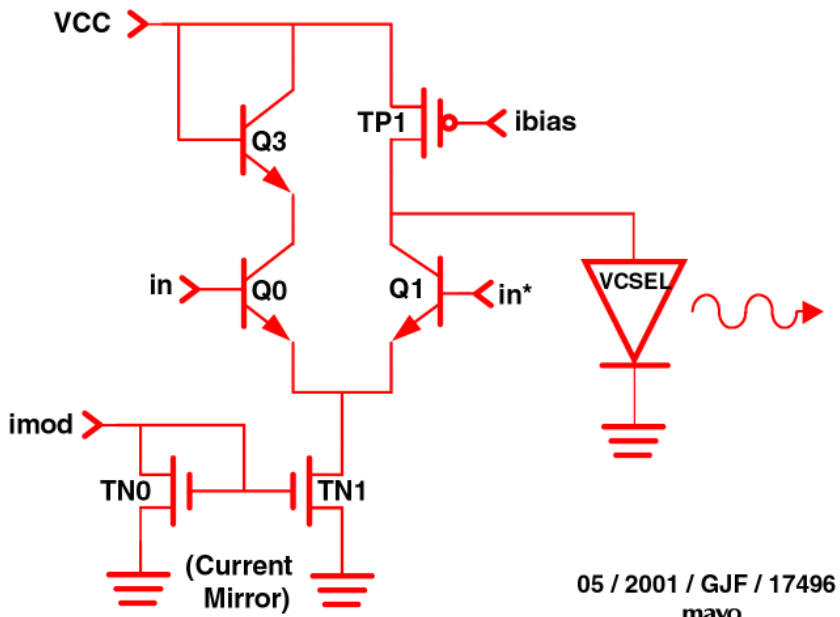
VOLTAGE - SOURCE AND CURRENT - SOURCE DRIVER CIRCUITS FOR DRIVING VCSELs IN A MULTI-Gb/s/CHANNEL FREE SPACE OPTICAL INTERCONNECTS DEMONSTRATION UNDER THE DARPA / MTO VLSI PHOTONICS PROGRAM

(Circuits Implemented in IBM SiGe 7 HP BiCMOS ASIC to be Heterogeneously Integrated with Honeywell GaAs VCSEL / Photodetector Array)

CURRENT SOURCE DRIVER
(TX: COURTESY OF UNIVERSITY OF DELAWARE)



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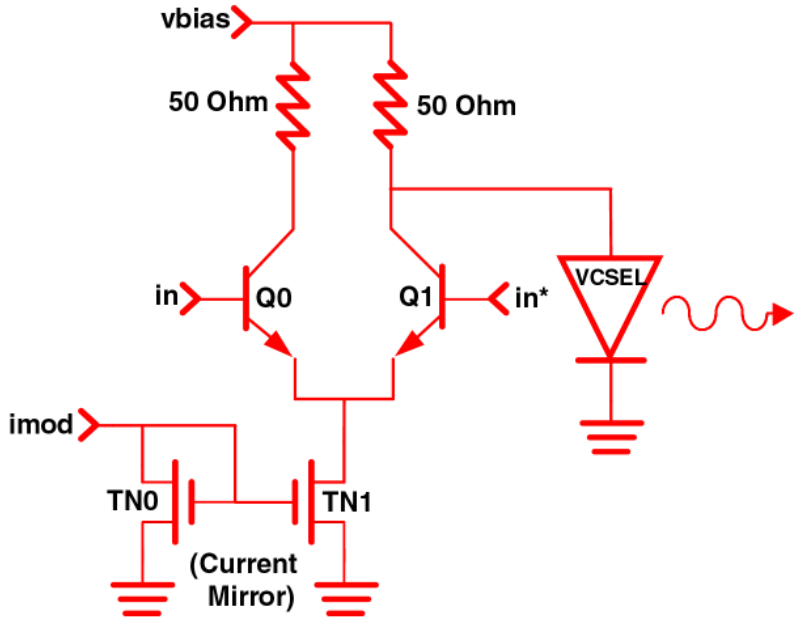
VOLTAGE SOURCE DRIVER
(TX)



For Current Source Driver:

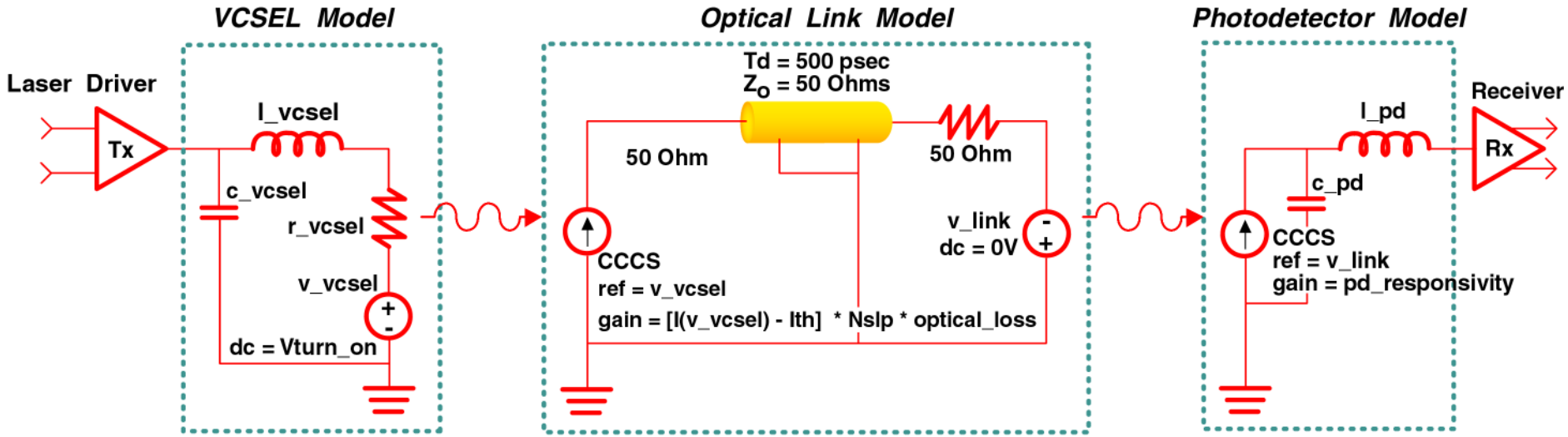
ibias = DC Bias Current Through VCSEL
imod = Modulation Current Through VCSEL
(Subtracted From ibias)
in, in= Differential Outputs From On-Chip Digital Buffer*
Simulated to 2 Gb/s. Limited by RC of VCSEL

For Voltage Source Driver:

vbias "Sets" DC Bias Current Through VCSEL
imod "Sets" Modulation Current Through VCSEL
in,in = Differential Outputs From On-Chip Digital Buffer*

Simulated to 8 Gb/s. Limited by RC of VCSEL.
50-Ohm Pull-Up Resistors Reduce Effective Load Resistance Resulting in Increased Bandwidth at Expense of Increased Power Consumption (e.g., Modulation Current Through VCSEL ~0.174 Imod)*

SIMULATION MODEL FOR OPTOELECTRONIC LINK IMPLEMENTED ON SMART PIXEL ARRAY (SPA) FOR MULTI-Gb / s / CHANNEL SiGe FSOI DEMONSTRATION (Each SPA Consists of ASIC Implemented in IBM SiGe 7HP BiCMOS Process Integrated with Honeywell GaAs VCSEL / Photodetector Array)



l_*, c_* = VCSEL / Photodetector Parasitics (Henrys, Farads)
r_vcsel = Slope of VCSEL IV Curve When VCSEL Is "On" (Volts/Amp)
I(v_vcsel) = Current Through VCSEL (Amps)
Ith = VCSEL Threshold Current (Current Required to Turn VCSEL "On") (Amps)
Nslp = Slope of VCSEL IP (Current vs. Optical Power Out) Curve When VCSEL Is "On" (Watts/Amp)
Vturn_on = VCSEL Anode Voltage When I(v_vcsel) = Ith. (Volts)
optical_loss = "Watts Into Photodetector" / "watts from VCSEL" (Watts/Watts)
pd_responsivity = Responsivity of Photodetector (Amps/Watt)
I(pd) = Current Through Photodetector (Amps)
CCCS = Current Controlled Current Source
Link gain = [I(v_vcsel)-Ith] *Nslp * Optical_Loss * pd_responsivity = 0.0224 Amps/Amp * [I(vcsel)-Ith]

Example: For [I(vcsel)-Ith] = 0.5 to 2.5 mA, I(pd) = 11.2 to 56 μA

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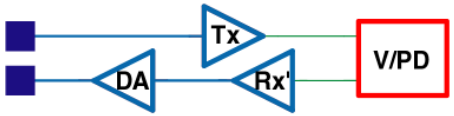
BLOCK DIAGRAM OF CIRCUITS IMPLEMETED ON IBM SiGe 7HP BiCMOS ASIC FOR MULTI-Gb / s / CHANNEL SiGe FREE SPACE OPTICAL INTERCONNECTS DEMONSTRATION (ASIC Contains Multiple Independent Optoelectronic Test Circuits for Evaluation at Up To 10 Gb / s / Channel)

Circuits 1-5 Are Replicated for Each of Four Clusters

Circuit 1: VCSEL / Photodetector Only

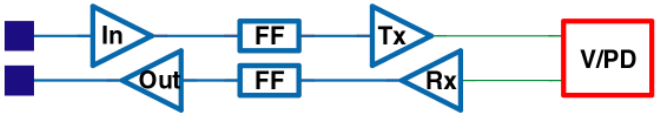
Circuit 2-3: Asynchronous Link

Circuit 2 = Voltage Source Tx
Circuit 3 = Current Source Tx



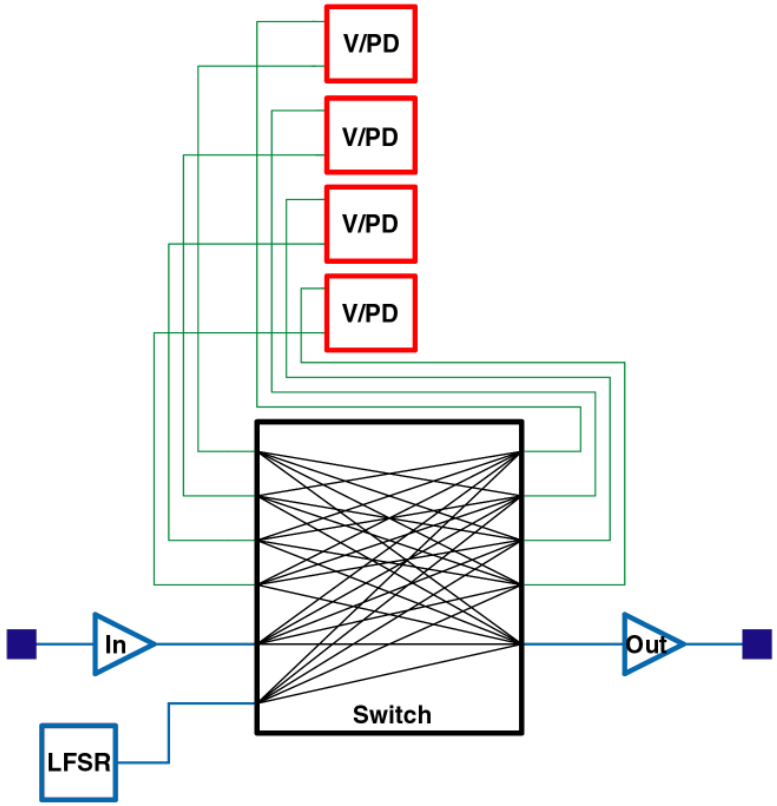
Circuit 4-5: Synchronous Link

Circuit 4 = Voltage Source Tx
Circuit 5 = Current Source Tx



Circuit 6-9: Synchronous Non-Blocking Crossbar Switch

(1 of 4 Channels Shown)



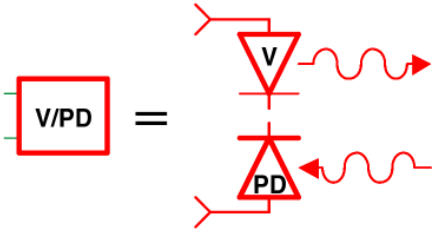
Legend

In = High Speed Differential Input Buffer
Out = High Speed Differential Output Buffer
DA = Differential Amplifier
Tx = Transmitter (Drives VCSEL)
Rx = Receiver (Receives from PD)
Rx' = Partial Receiver (Used in Async Circuits)
V = VCSEL
PD = Photodetector
FF = Flip Flop
LFSR = On-Chip Linear Feedback Shift Register

Single-Ended Signal

Differential Signal

Pair of ASIC I/O Pads for Differential Signals In or Out



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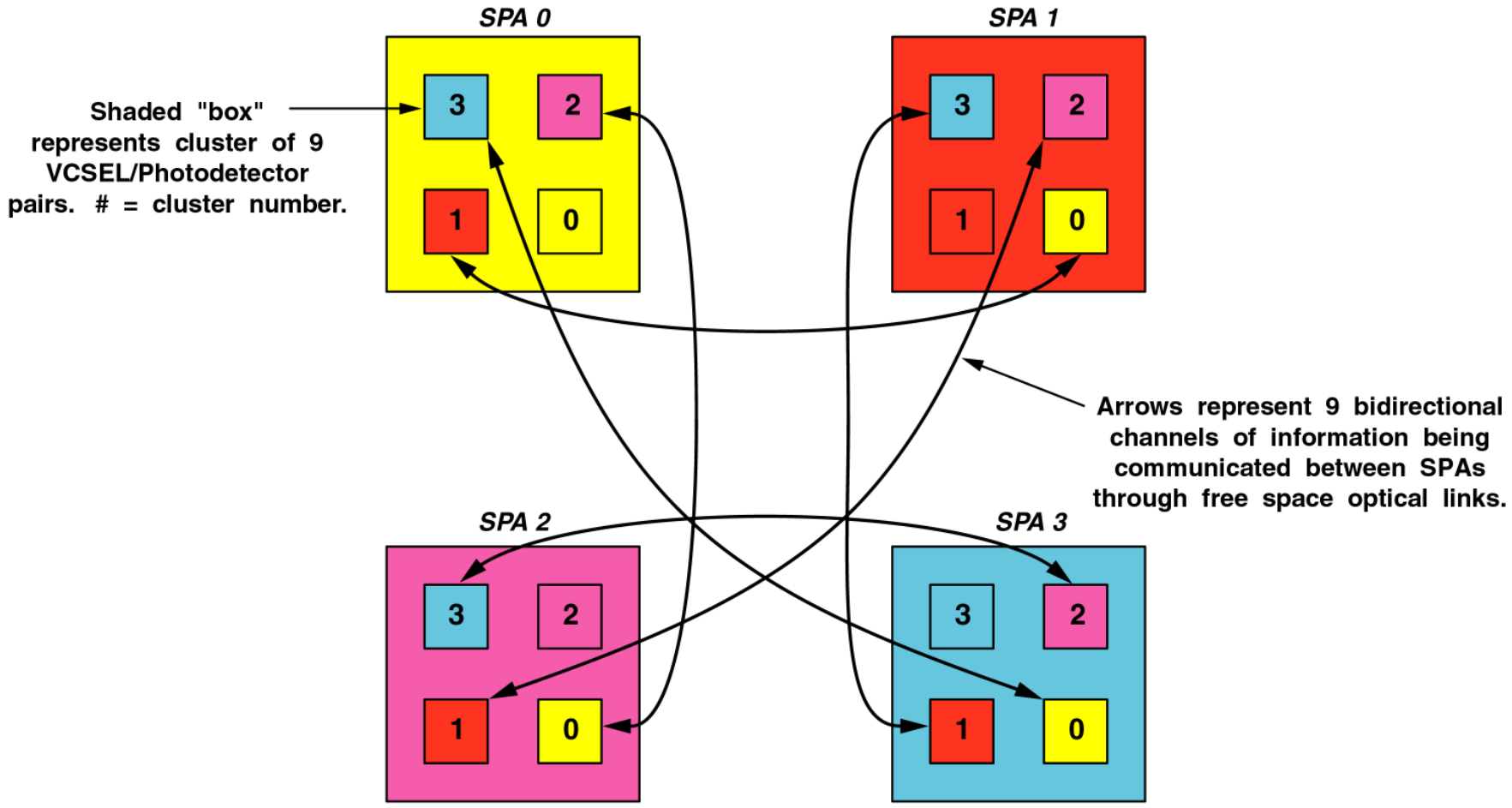
SPA-TO-SPA CLUSTER MAPPING FOR MULTI-Gb/s/CHANNEL SiGe FREE SPACE OPTICAL INTERCONNECTS DEMONSTRATION

(Each SPA Consists of ASIC Implemented in IBM SiGe 7HP BiCMOS Process Integrated With Honeywell GaAs VCSEL/Photodetector Array; Each GaAs Array Has Four Active Clusters of 9 VCSELs and 9 Photodetectors Each)



Note: SPA-"x"/cluster-"y" communicates with SPA-"y"/cluster-"x". SPA-"x"/cluster-"x" communicates with itself. This mapping is color coded: light blue clusters communicate with the light blue SPA, red clusters communicate with red SPA, etc. For an "n"-SPA system, there must be at least "n"-clusters symmetrically arrayed on each SPA to accommodate the optical lens system.

SPA = Smart Pixel Array

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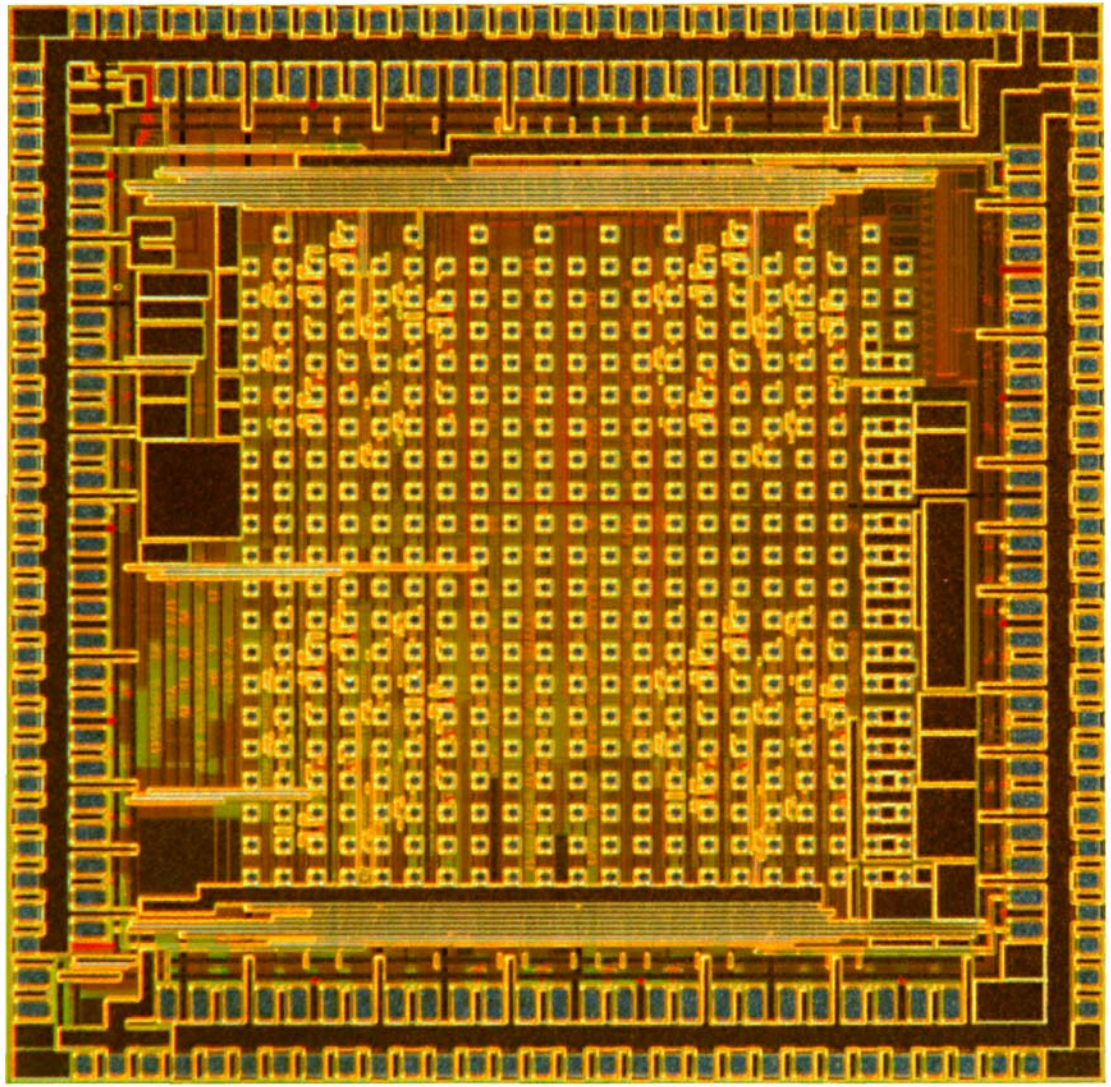
PHOTOGRAPH OF SMART PIXEL ARRAY ASIC DESIGN IMPLEMENTED IN IBM SiGe BiCMOS 7HP PROCESS (0.18 μm CMOS FETs, 120 GHz f_T HBTs) FOR DARPA / MTO VLSI PHOTONICS PROGRAM

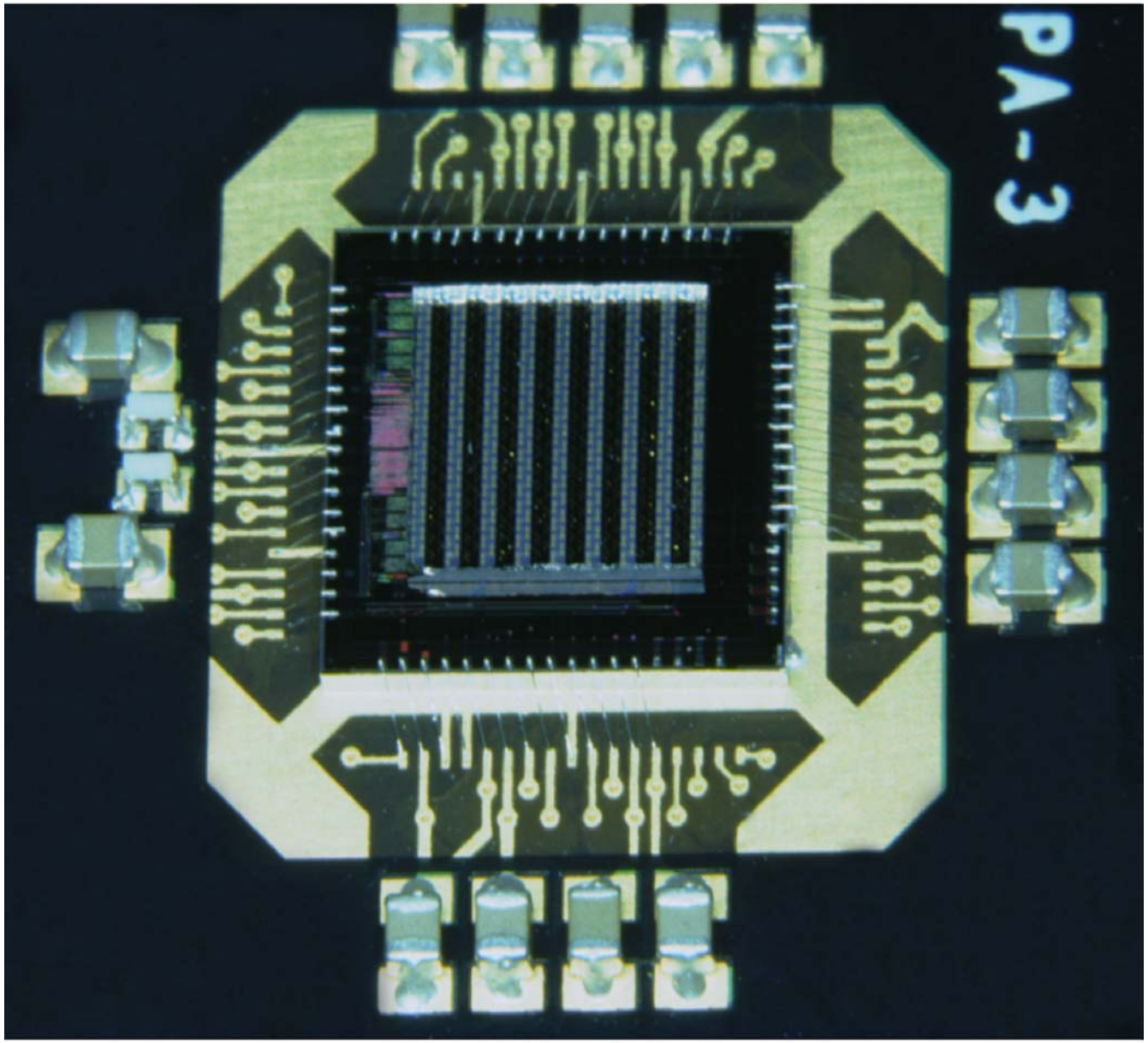
(View of Entire ASIC; 4.2 x 4.2 mm Die; Fabricated in Mayo / SPAWAR Multi-Project Wafer Run #2 [MPW-2])



06 / 2001 / GJF / 17701

mayo

OBLIQUE PHOTOMICROGRAPH OF SMART PIXEL ARRAY (SPA) ASSEMBLED ONTO FASTNET MCM



08 / 1999 / GJF / 16395

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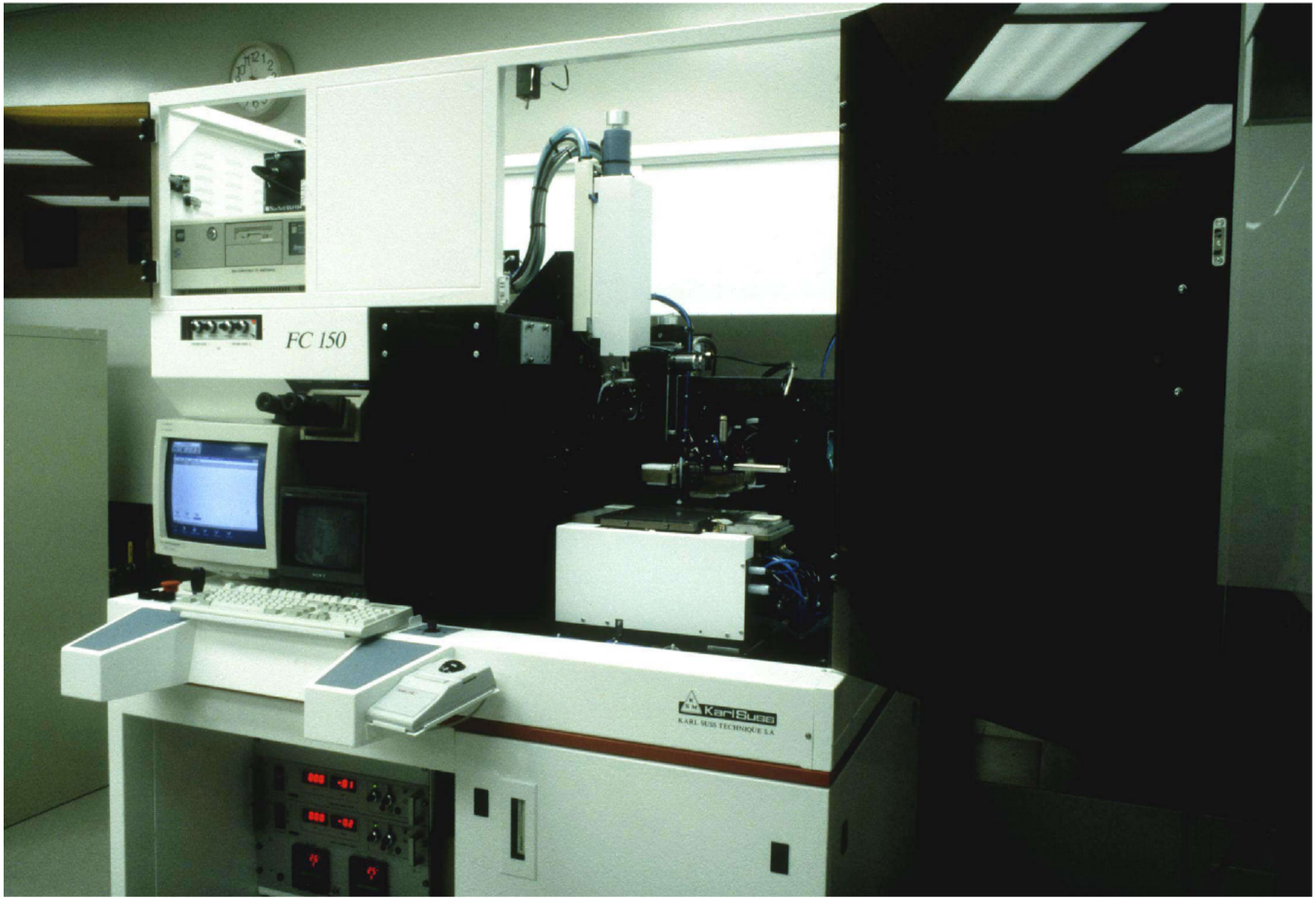
PRECISION ASSEMBLY TECHNOLOGY FOR SPA PLACEMENT

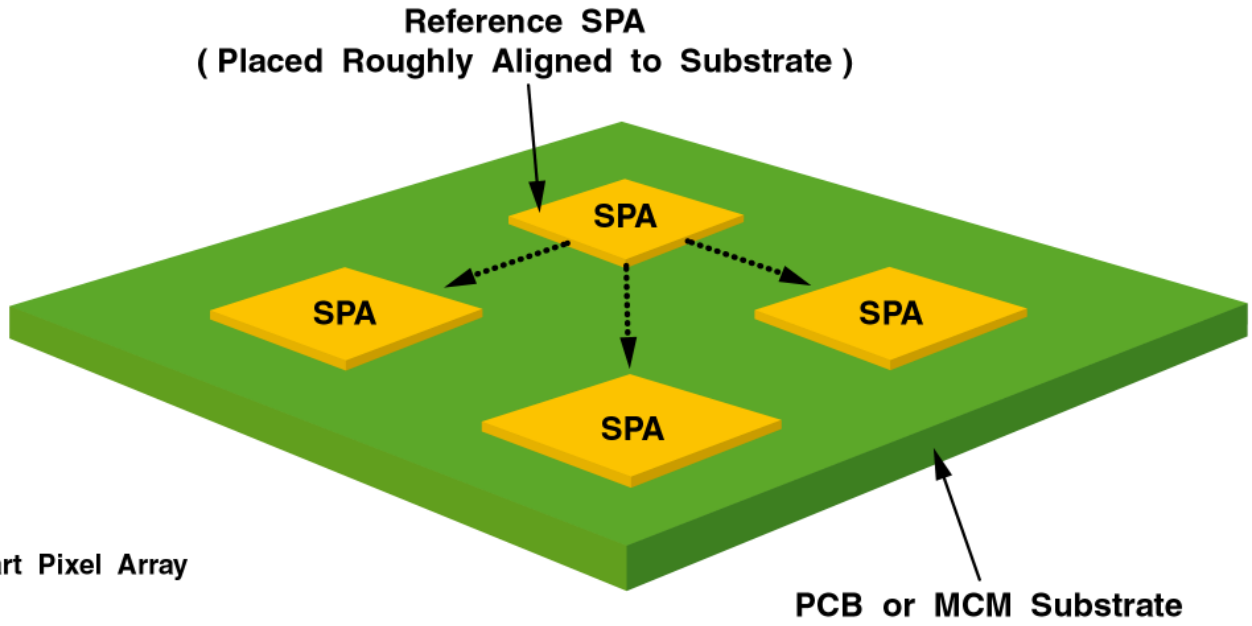
- Mayo precision assembly method allows for face-up die attach of smart pixel arrays
  - Useful for quick-turn prototypes
  - Passively aligned
  - Allows for low-cost substrates

KARL SUSS FC - 150 FLIP CHIP DIE BONDER



03 / 98 / MEV / 12752

BLOCK DIAGRAM OF MAYO PRECISION SMART PIXEL ARRAY ASSEMBLY PROCESS DEVELOPED UNDER DARPA FSOIA PROGRAM AND USED IN VLSI PHOTONICS PROGRAM
(Utilizes Karl Suss FC-150 Flip Chip Bonder for Face-Up Die Attach)



- Subsequent SPAs Placed "Relative" to Reference SPA (+/- 10 μm Accuracy, +/- 5 μm Achievable)
- SPA-to-SPA Alignment Based on Alignment Marks on SPAs, Not Substrates
- Electrical Connections to Substrates Can Be Through Wire-Bonds or Contacts on Back of SPAs

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MILESTONES / TECHNICAL ACCOMPLISHMENTS

- Designed and delivered 4-channel sychronous Tx and Rx die to Northrop Grumman for their interim demonstration. Fabricated in Honeywell 0.35um CMOS SOI process.

- Initial signal integrity, mechanical and thermal analysis performed on critical sections of VIVACE team system. MCM design started.

- SiGe ASIC designed for high per-channel data rate demonstration. Fabricated in IBM SiGe BiCMOS 7HP process. SiGe demonstration MCM design started.